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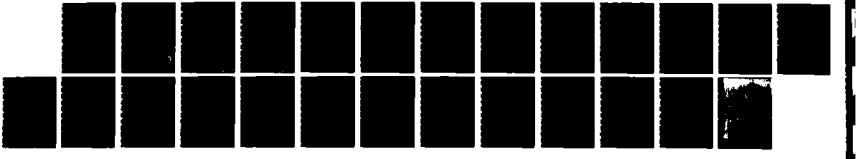

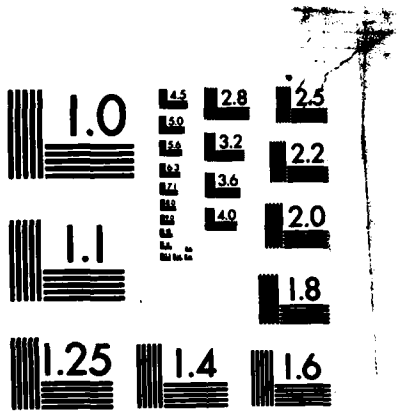

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DEFECTS AT ELECTRODE OXIDE AND ELECTRODE SILICON INTERFACES IN VHSI DEVICE STRUCTURES

FINAL REPORT

C. R. HELMS, M. A. TAUBENBLATT,
P. W. LEW, AND J. D. PLUMMER

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STANFORD ELECTRONICS LABORATORIES
STANFORD UNIVERSITY
STANFORD, CALIF. 94305

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The effect of impurities on the electrical properties of metal silicon interfaces has been investigated for Pt, Ta, Ti, Hf, and their silicides. These silicon-electrode systems are of critical importance in VHSIC and other VLSI systems. The impurities investigated include oxygen (as in SiO_2 or metal oxides), carbon, and silicon dopants. In order to quantitatively determine the effect of these impurities on the electrical properties of the nutral silicon interface microanalysis measurements have been combined in situ with over→

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measurements of Schottky barrier height via internal photoemission. Using this combination of techniques, the interface chemical composition can be determined and related to the measured Schottky barrier height. With a few exceptions, we have found that reliable, reproducible, Schottky diodes on silicon can only be formed if the metal silicon structure is annealed above the silicide formation temperature, so that the silicide formation reaction can "clean up" the interface. In addition, we have determined the mechanism for the poor reproducibility in barrier height for a number of refractory metal silicon contacts which is related to thin oxides that may be present at the interface.

Table of Contents

Illustrations

I. Introduction

The backbone of current LSI/VLSI technology and the next generation of VHSI technology is the n-channel silicon gate MOS transistor. In order to reduce device dimensions below 1 μm lateral line widths, however, new limitations on device performance must be considered. Some of these limitations are inherent in the device scaling process, but many are associated with defects present in the device structure; some of these defect-related limitations have been addressed in this program. One example of this is the reported difference in the physical, electrical, and optical properties of very thin (<200 Å) oxide layers compared to thicker layers. Of critical importance for VHSI MOS devices is the effect of these thin oxides on the charges present at the Si-SiO_2 interface. As another example, the resistivity of polycrystalline silicon used in current NMOS technology cannot be scaled low enough to be used in submicron circuits. New electrode materials, such as refractory metal silicides, with low resistivities are being used for this purpose. Interfacial defects associated with these new interconnect materials may be a prime component in determining device performance.

In this program, we have primarily investigated the effect of interfacial impurities on the properties of ohmic and Schottky contacts for a selected number of electrode systems.

The basic approach of this program was to apply interface microanalysis to investigate the chemical nature of the silicon metal interface and electrical characterization of the same specimens so that changes in electrical properties could be directly related to chemical changes at the interface. This approach is absolutely necessary, and we have developed a measurement system where interface microanalysis can be accomplished and Schottky barrier height measurements made (using internal photoemission) in situ in the same system.

This has made possible a direct comparison of the Schottky barrier height with the metal-silicon inerface chemistry on exactly the same specimen in real time.

The above studies apply equally well to Schottky or ohmic contacts. Schottky contacts are of great importance for current bipolar technology and for VHSI technology utilizing MESFETs. Although VHSI MESFET technology is in its infancy, it may offer substantial advantages over NMOS technology for some applications [1,2]. Since it uses a Schottky-barrier gate, MESFETs are a low voltage technology. This has been unattractive in the past; however, since VHSI NMOS voltages scale inversely as lateral device dimensions, operating voltages in NMOS and MESFET devices will be comparable for submicron geometries. The MESFETs major advantage lies in the replacement of the MOS capacitor with a Schottky-barrier contact which provides more speed and potentially better yield due to the elimination of oxide pinholes and interface fixed charge. Many of the results obtained in this program have formed the basis for the development of complimentary MESFET structures, which we are currently developing with support from the Semiconductor Research Corporation.

II. Statement of the Problem

As stated above, defects and impurities play an important role in determining the properties of silicon-metal contacts. Especially for the refractory transition metals, the reproducibility of the Schottky barrier height to silicon is typicaly not sufficient and in many cases is no better than ±0.1 eV. This poor reducibility appeares to be related to the nature of impurities present at the metal/silicon interface.

With this in mind, we began this program with the goal of determining the effect of specific impurities purposefully introduced at the silicon metal interface on the electrical properties of the interface, specifically the Schottky barrier height. More specifically, we have limited our investigations to Ta, Ti, Hf, and Pt layers on silicon and to interfacial impurities, including dopants, oxygen, and carbon.

Pt was chosen since it is a commonly used electrode material for high barrier Schottky contacts to n-type silicon. In addition, as used for these devices, the Pt is reacted with the silicon at relatively low temperatures to form a silicide/silicon interface very clean with respect to common silicon surface impurities such as carbon or oxygen. Ta, Ti, and Hf were chosen as they represent candidate electrodes for lower barrier contacts to n-type silicon or high barrier contacts to p-type silicon. The impurities carbon and silicon were chosen as they are the common extrinsic impurities present on the silicon surface prior to metal deposition and at the silicon metal interface. Dopants at the silicon metal interface can be important due either to segregation effects at higher temperatures or the so-called snowplow effect during silicide formation.

III. Significant Results and Accomplishments

A list of significant results and accomplishments follows. A more detailed description of Items 1, 4, and 5 appears in Section IV.

(1) Determined that reproducible, reliable, metal contacts to Si occur only if the interface formed is free of extrinsic impurities, such as carbon and oxygen. For Si surfaces present in device structures, thermal annealing at T > silicide formation temperature is necessary (see paper #1, 4, 5 and report #2).

(2) Observed out diffusion of As through platinum silicide at low temperatures, suggesting that the electrical properties of these contacts will not be stable for subsequent thermal anneals (see report #2).

(3) Established that increases in the barrier height to ultra-clean silicon surfaces of up to 0.3 eV could be produced by surface doping (see report #1).

(4) Quantitatively determined the effect of common wet chemical cleaning procedures on Si surface chemistry; determined the effect of the surface contaminants on barrier heights (see paper #5).

(5) Settled long standing controversy concerning the barrier height of Hf to Si; accurately determined the barrier height and the effect of thin oxides (see paper #5).

(6) Investigated the thermo-chemical properties of Si-O-Ti interfacial systems; showed that the chemistry of Ti-SiO_2-Si layers could be predicted from bulk thermodynamica (see paper #2 and 5).

IV. Detailed Findings

Since the results and accomplishments listed above are described in detail in previously supplied reports and reprints, all of our significant results will not be discussed in any detail. However, Items 1, 4, and 5 are particularly significant and will be discussed in more detail here.

1. Formation of Reliable, Reproducible Contacts

It is now well established, from our work as well as others, that reliable, reproducible contacts to silicon can only be formed if the final interface present is free from impurities. This can be accomplished by sputtering and high temperature annealing of the silicon surface prior to metal deposition. This procedure is not, however, compatible with typical IC processing schemes. Sputtering alone is also not desirable due to the damage created and the possible inclusion of inert gasses. For present day technology, the most appropriate method to achieve the clean interface condition is to anneal the system above the silicide formation temperature so that interfacial reaction will occur, "cleaning up" the interface. Figure 1 shows the transition metal region of the periodic table with the appropriate silicide formation temperatures indicated. For the more noble metals on the right hand side, the silicide formation temperatures are low enough so that silicide can be easily formed for temperatures consistent with post metallization annealing for typical IC processes. Most of these metals have barriers to n-type silicon >0.7 eV. For lower (higher) barriers to n- (p) type silicon, the choices lie to the left of the table. Although the Column III metals Si, Y, and La, as well as the rare earths, all have low barriers to n-type Si and lower silicide formation temperatures, they also form stable oxides and are very corrosion sensitive, and thus poor choices for IC fabrication. Of the metals remaining, only Ti and Hf have silicide formation temperatures low enough to be compatible with most post metalization IC processing. Therefore, these metals, Ti and Hf (or alloys containing them, such as Ti-W), appear to be the best choices for low (high) barrier contacts to n- (p) type silicon.

Another method which may prove feasible is the deposition of the appropriate metal, using CVD techniques with flourine or chlorine present. These

reactive gasses will etch the Si surface and may provide a more ideal clean metal-Si interface without silicide formation.

2. Interface Effects in Ti and Hf Schottky Barriers on Silicon

Titanium and hafnium Schottky barriers are of interest in integrated circuit and photovoltaic technologies and for theoretical study, due to their reported anomalously high (low) barriers to p-type (n-type) silicon [3-7]. Spectroscopic studies in this laboratory [8] and others [6,9-12] have shown that Ti and Hf do not form silicide until relatively high temperatures ($TiSi_2$ at 500°C, HfSi at 550°C, and $HfSi_2$ at 750°C), although considerable intermixing can occur at temperatures well below this [12]. They have relatively high heats of formation and react with SiO_2 and carbon to form metal oxides and carbides.

Previous studies [3-7, 11, 13-15] have reported a variety of values for barrier height for these metals and their silicides for samples prepared using a variety of processing procedures. In those studies, the level and nature of contamination on the silicon surface prior to metal deposition and that accrued during metal deposition and post metalization anneals were not well determined or controlled, making it difficult to assertain the important factors contributing to the barrier height values obtained.

In order to determine the effect of interface chemistry in a rigorous way, we have developed a UHV analysis system capable of in situ internal photoemission measurement of barrier height, in addition to surface analysis (Auger, photoemission spectroscopies, etc.) and sample preparation (annealing to 1000°C, cooling to -150°C, sputtering, metals

evaporation, and gas exposures). A novel scheme employing WSi_2 as a back-side contact, as well as a front side contact, to the thin (≈100 Å) metal layer is used to ensure stability after high temperature anneals. This contact pad arrangement allows good ohmic contact to the diode and is stable for anneals greater than 1000°C. Preparation of the diodes in UHV is critical for the control and determination of contaminants. In addition, measurement of the barrier in situ is advantageous for a number of reasons. Post deposition processing, such as annealing, which is critical for typical device fabrication, can be easily done on the same sample. No contamination can occur from gas exposure or diffusion, which is especially important during anneals. And, finally and most importantly, the surface and interface may be monitored with spectroscopic tools before and after metal deposition and anneals at the same time that barrier measurements are made.

During a typical experiment, the surface is prepared in the desired manner, characterized using surface spectroscopies, and approximately 100 Å of the metal is then deposited using e-beam evaporation. The barrier is then determined by internal photoemission, using front side illumination over a photon energy range of 0.6-1.0 eV. The yield (electrons collected per photon) can be described by $Y = C_1(h\nu-\Phi_b)^2/h\nu$ [16]. This equation accounts for a proper normalization of adsorbed photons not present in the more commonly used Fowler equation, $Y = C(h\nu-\Phi_b)^2$ [17], and gives an improved fit, especially for low barrier heights and a slight increase in calculated barrier height (≈0.02 eV) in this energy range.

In the studies reported here, we have investigated the Ti-Si system in detail for the following sample types. Starting material in all cases was Si (100) $10^{16}/cm^3$:

(1) Clean Si (100) prepared by sputtering and annealing (900°C) vs post metal annealing temperature, p- and n-type.

(2) Si (100) chemically prepared using the RCA clean [18] without the final HF step, p- and n-type, vs post metal annealing temperature, p-type.

(3) Si (100) chemically prepared using the RCA clean vs post metal annealing temperature, p-type.

We have also studied Hf deposited on sample types 2 and 3 above for low temperature anneals and on p-type using both internal photoemission and I-V measurements.

In order to relate observed barrier heights to known integrated circuit chemical cleaning procedures, the effect of surface preparation on surface contaminant levels was determined using Auger electron spectroscopy. Auger spectra from the Si surface is shown in Fig. 2 for two common procedures, the RCA clean with and without the final HF dip. The RCA clean, after air exposure, leaves approximately one monolayer of carbon and approximately one half monolayer of oxygen. If the HF dip is omitted, a surface with a thin SiO_2 layer of two to three monolayers and less than 0.2 monolayers of carbon is produced. The presence of the thin oxide on the surface prepared by the RCA clean without the HF dip is also evidenced by the major change in the Si LVV lineshape, consistent with 2-3 monolayers of SiO_2 on the surface. It is interesting to note that ellipsometer thickness measurements of these oxides give much larger values for the thickness, definitely inconsistent with the large substrate component present in the LVV spectra.

The barrier height of Ti deposited on clean Si (100) p- and n-type Si prepared by in situ sputtering and annealing and on samples prepared by the RCA

clean with HF as a function of annealing temperature is shown in Fig. 3. These barrier heights were determined from internal photoemission to ±0.01 eV and are uncorrected for image force or tunnel lowering. A typical internal photoemission spectrum is shown in the insert, where $(Y\ h\nu)^{1/2}$ vs $h\nu$ is plotted for a $TiSi_2$ barrier formed by annealing Ti deposited on clean Si (100) to 500°C. We find, for the Ti-Si system, that the initial barrier to clean, n-type, sputter annealed (900°C) Si is 0.51 eV. This barrier varies only slightly for anneals below 500°C, even though considerable intermixing between Ti and Si occurs [12]. The barrier increases sharply to 0.58 eV for anneals above this temperature when $TiSi_2$ is formed (as verified by Rutherford backscattering). These results are similar to those obtained by Kato and Nakamura [11] for Ti films sputtered onto chemically cleaned Si. However, this behavior is markedly different than that of V [19], where it is found that the barrier stabilizes at the silicide value during the intermixing phase which is at much lower temperatures (350°C). On p-type Si, the initial barrier is 0.60 eV which varies only slightly for anneals up to 800°C.

The RCA clean, without an HF dip which has a thin interfacial oxide present, shows a high barrier to p-type of 0.72 eV and a correspondingly low barrier on n-type of 0.3 eV. Annealing at 300°C causes this high barrier on p-type to decrease to 0.63 eV. It continues to decrease until silicide is formed, in agreement with the silicide value for a clean starting surface. For samples prepared using the full RCA clean, where minimal oxygen was present, a barrier height similar to that on clean Si is obtained. This value of the barrier height is in agreement with that of Cowley [3] for a similar surface preparation, although measurement of the interface contamination levels were not made in that study. Our I-V measurements on Ti p-type diodes prepared in UHV and measured ex situ show a barrier of 0.72 eV

(n = 1.1) to samples prepared with an RCA without HF clean and 0.56 eV (n < 1.3) for an RCA clean, in good agreement with the in situ internal photoemission measurements. The behavior of the barrier heights for the Ti-Si system can be understood in terms of the thermodynamics of the Ti-O-Si system [8]. For thin layers on the order of a monolayer concentration, the Ti will react with the oxide forming Ti oxides plus silicon and possibly Ti silicide. This allows reasonably intimate contact between the Ti and Si, giving a value of barrier height similar to the clean surface values. For thicker oxides (still only 2-3 monolayers!), the Ti will still react with the surface but apparently does not penetrate through the oxide, giving a barrier height no longer representative of the Ti-Si interface. Upon annealing, the kinetics of the Ti-SiO_2 reaction is accelerated so that ultimately intimate contact between Ti or Ti silicide and Si is again achieved.

The results of Hf metal on p-type Si are similar to those found for Ti. These barriers were prepared in UHV and measured ex situ using both internal photoemission (PR) and I-V. Diodes prepared with several monolayers of SiO_2 show a barrier of 0.66 eV for both PR and I-V with an ideality factor (n) of 1.05 and excellent reproducibility. This barrier decreases to 0.56 eV when heated to 200°C (in N_2). Diodes prepared with the RCA clean have a lower barrier of 0.54 eV from PR and 0.56 eV for I-V with an ideality factor of 1.06-1.12.

None of our sample preparations produced a barrier as high as the reported 0.9 eV on p-type silicon for Hf [4-6] or Ti [7]. In these previous studies, the metal was either sputter deposited or evaporated in a relatively poor vacuum (10^{-6} torr). A surface preparation similar to the RCA clean was used, with the exception of [7] where a RCA without HF was used and an anneal of 520°C was required to produce a high barrier. Lower barriers in the Hf-Si

system were found in this work and by Beguwala [13], where the Hf was deposited by e-beam evaporation in a superior vacuum (10^{-8} torr). One exception to this is [14], where a low barrier was found for sputter deposited Hf. However, in this study, the Si surface was first sputter cleaned without annealing, which we have found can significantly change the barrier height, and the substrate reached a temperature of 200°C during deposition, which we have shown is high enough to cause significant changes in the barrier height due to metal reaction with the interfacial impurities. In those studies reporting high barrier heights, the diodes were prepared by methods with unknown levels of contaminants, and the presence of additional contaminants (such as hydrogen) may be responsible. Another explanation may be the presence of a thicker insulating layer consisting of SiO_2 and metal oxides, carbides, or hydrides which may be present on the Si surface initially or resulting from interfacial segregation of impurities in the metal film during annealing.

Nevertheless, interfacial SiO_2 does increase (decrease) the barrier of these metals to p-type (n-type) silicon by >0.1 eV. The barrier height measurements are very sensitive to low barrier regions, and we observe no additional tails for the yield plots on the high barrier samples indicating a nearly continuous layer is present. The effect of interfacial oxides on barrier height has been explained by Turner and Rhoderick [20] as due to a reduction in the Si interface states due to oxygen bonding to Si. This results in a reduction, in turn, of the pinning ability of the states, so that the barrier behaves more like an ideal Schottky barrier with low work function metals having high (low) barriers to p-type (n-type) silicon. Card and Rhoderick [21] have analyzed the effect of an interfacial oxide layer theoretically using I-V and C-V measurements. A small increase in barrier height due to tunneling is expected for both n- and p-type silicon. A larger shift

in barrier height predominated, though, and was attributed to fixed oxide charge. Positive oxide charge (as is usually observed in MOS devices) would account for an increase in the barrier to p-type. However, one would expect oxide charge of this nature to be relatively independent of the metal, whereas the barrier shifts seem to vary with metal work function as reported by Turner and Rhoderick [20]. An effective average work function due to microclusters of varying phase as proposed by Freeouf [22-24] may also explain the observed behavior. An increased barrier to p-type would require titanium oxide phases to have a work function less than that of titanium silicide phases. Experimental data [25], however, indicates a relatively high work function for TiO_2 (5.7 eV) compared to that of Ti (4.33 eV) [26], Si (4.85 eV, cleaved (111)) [27] and the probable work functions of titanium silicides. In addition, low barrier regions representative of more intimate silicon-titanium junctions would also be expected. Since we observe no such low barrier regions, if they are present at all, their physical extent must be much less than the silicon Debye length (400 A for $10^{16}/cm^3$ doping).

The increased (decreased) barrier to p-type (n-type) silicon occurs only if several monolayers of SiO_2 are present. In fact, it is remarkable that only a few monolayers of SiO_2 is sufficient to produce the high p-type barriers observed. For contamination of order of a monolayer, Ti reacts to form Ti-O complexes [6,10] which could remove the passivating effect of the Si-O bonding or the fixed charge, resulting in a barrier similar to that on the clean surface. The nature of the Ti-Si bonding is also important, since the barrier to n-type Si varies little from the as deposited value until silicide is formed even though considerable intermixing of the Ti and Si is occuring.

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Sc --	Ti 500	V 600	Cr 400	Mn 400	Fe 450	Co 350	Ni 200	Cu --	Zn
Y 350	Zr 700	Nb 650	Mo 525	Tc --	Ru --	Rh 377	Pd 100	Ag	Cd
La --	Hf 550	Ta 650	W 650	Re --	Os --	Ir 400	Pt 200	Au	Hg

Fig. 1. Lowest temperature of silicide formation.

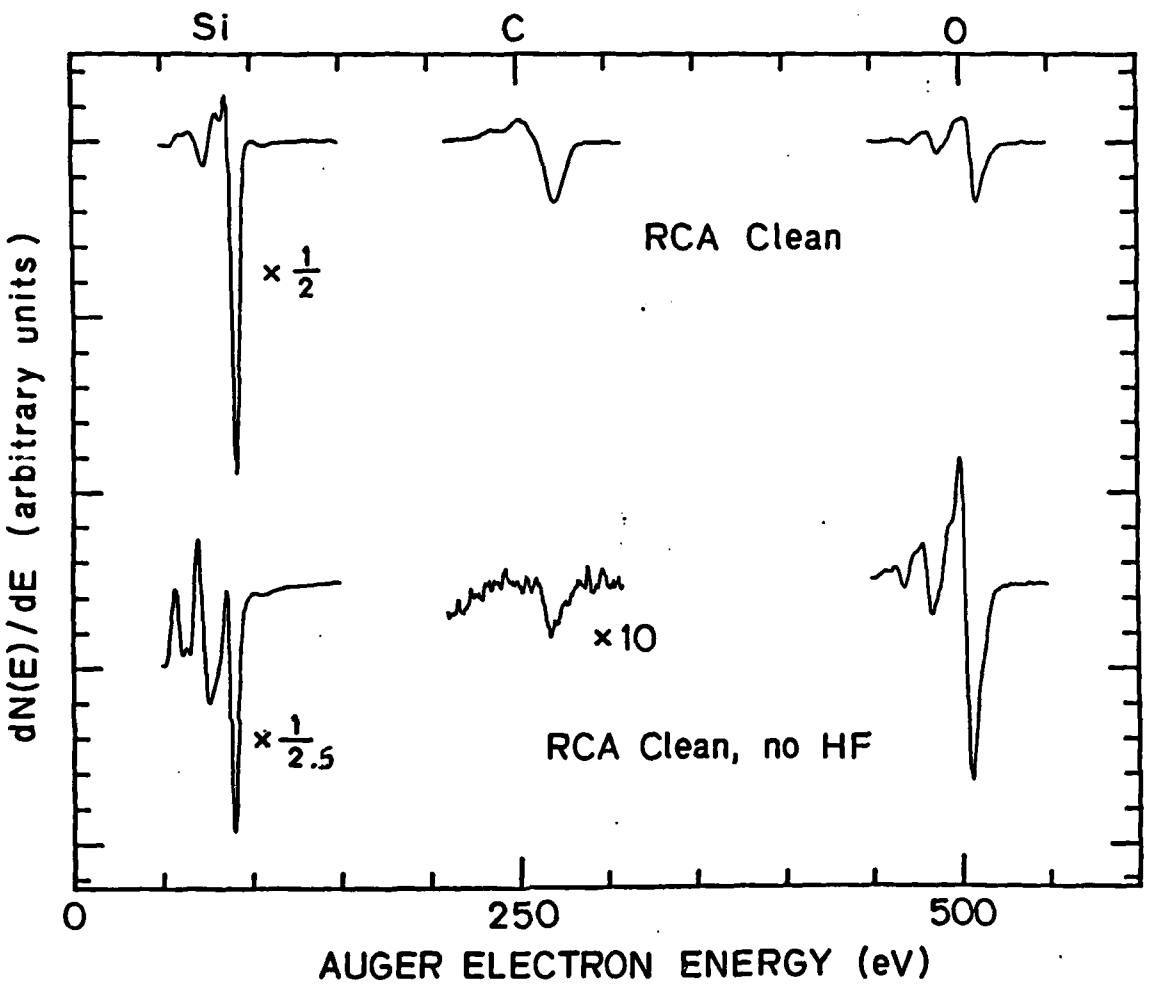

Fig. 2. A comparison of chemical cleaning procedures using Auger electron spectroscopy. The RCA clean leaves approximately one monolayer of carbon and one half monolayer of oxygen. Omitting the final HF dip from the procedure leaves two to three monolayers of SiO_2 and less than 0.2 monolayer of carbon.

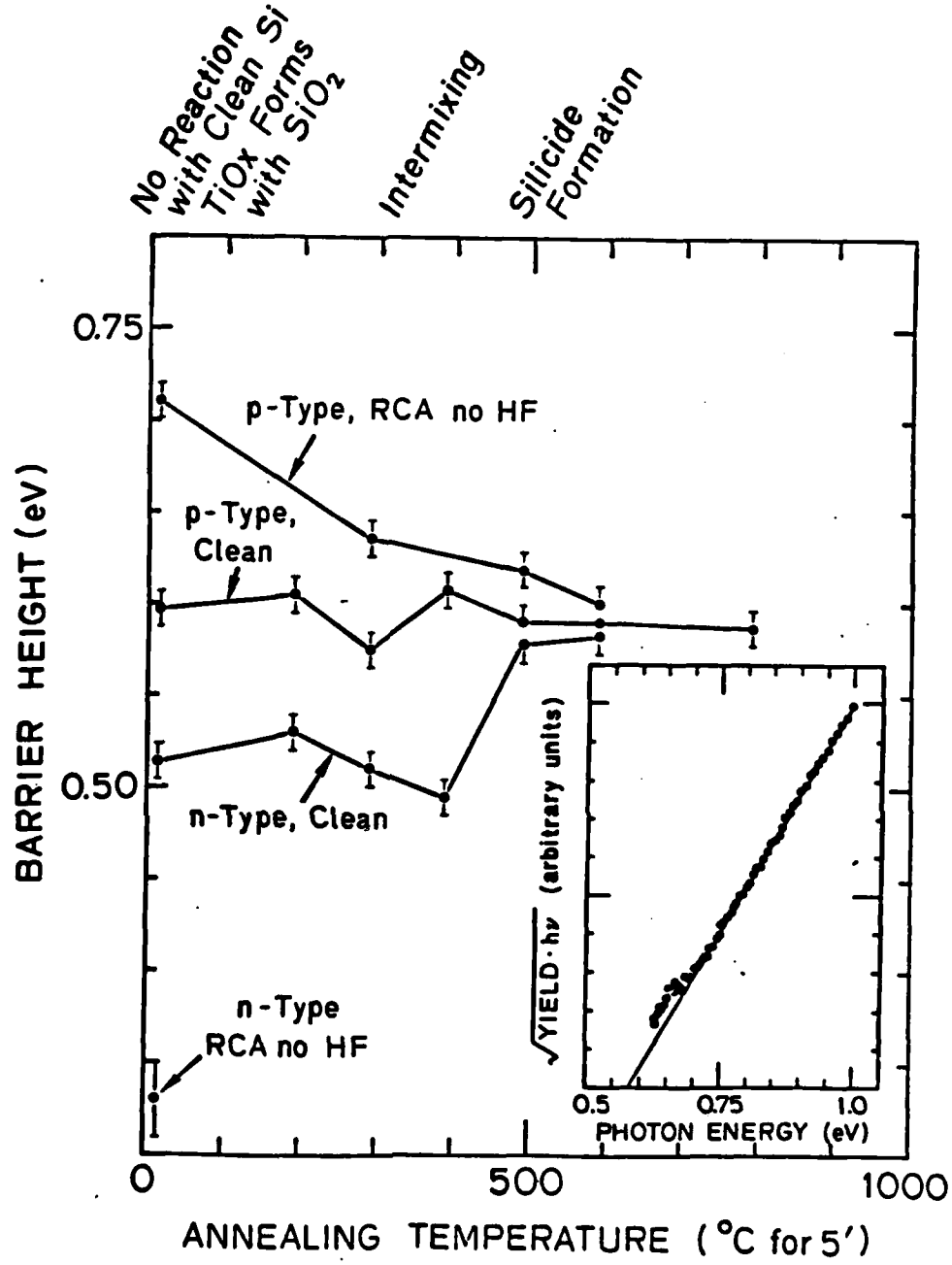

Fig. 3. Schottky barrier height on clean Si (100) prepared by sputtering and annealing (900°C) and on Si with 2 to 3 monolayers of SiO_2, prepared using the RCA clean with no final HF dip vs post metalization annealing (5') temperature for p- and n-type silicon. Various regions of interaction have been determined from spectroscopic studies as noted. Insert: Internal photoemission data, $TiSi_2$ barrier formed by 500°C anneal on clean p-type Si, $(Y\ h\nu)^{1/2}$ vs $h\nu$, x-intercept gives Φ_b.

List of Publications and Technical Reports

Publications:

1. P. W. Lew and C. R. Helms, "Summary Abstract: Effect of Interfacial Impurities on Tantalum-Si Schottky Barrier Structures," J. Vac. Sci. Technol. 20, 691 (1981).*

2. M. A. Taubenblatt and C. R. Helms, "Silicide and Schottky Barrier Formation in the Ti-Si and the Ti-SiO_x-Si Systems," J. Appl. Phys. 53, 6308 (1982).

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Technical Reports:

1. S. C. Perino, "The Electronic Structure and Deposition Kinetics of Arsenic on the Si Surface," SEL Report J302-1, Stanford Electronics Laboratories, Stanford University, September 1982.***

2. P. W. Lew, "Reproducibility and Stability of Ta, Ti, and Pt, Silicide Contacts to Si," SEL Report J301-1, Stanford Electronics Laboratories, Stanford University, March 1983.*

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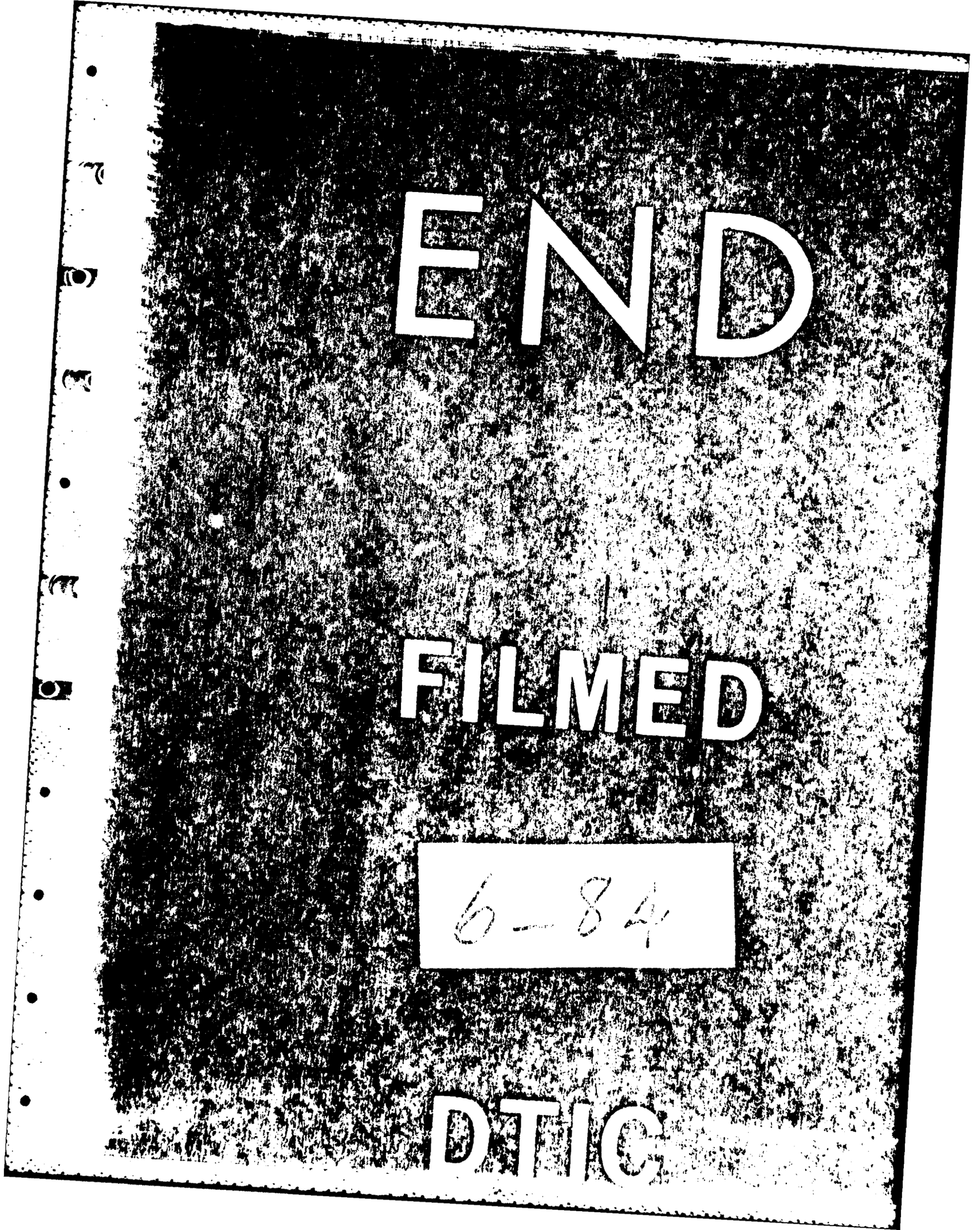
List of Participating Scientific Personnel

1. Professor C. R. Helms, Principal Investigator
2. Professor J. D. Plummer, Co-Investigator
3. Dr. S. C. Perino, received degree September 1982, now at Tektronix
4. Dr. P. W. Lew, received degree March 1983, now at IBM
5. Mr. M. A. Taubenblatt, Research Assistant
6. Mr. A. Akinwande, Research Assistant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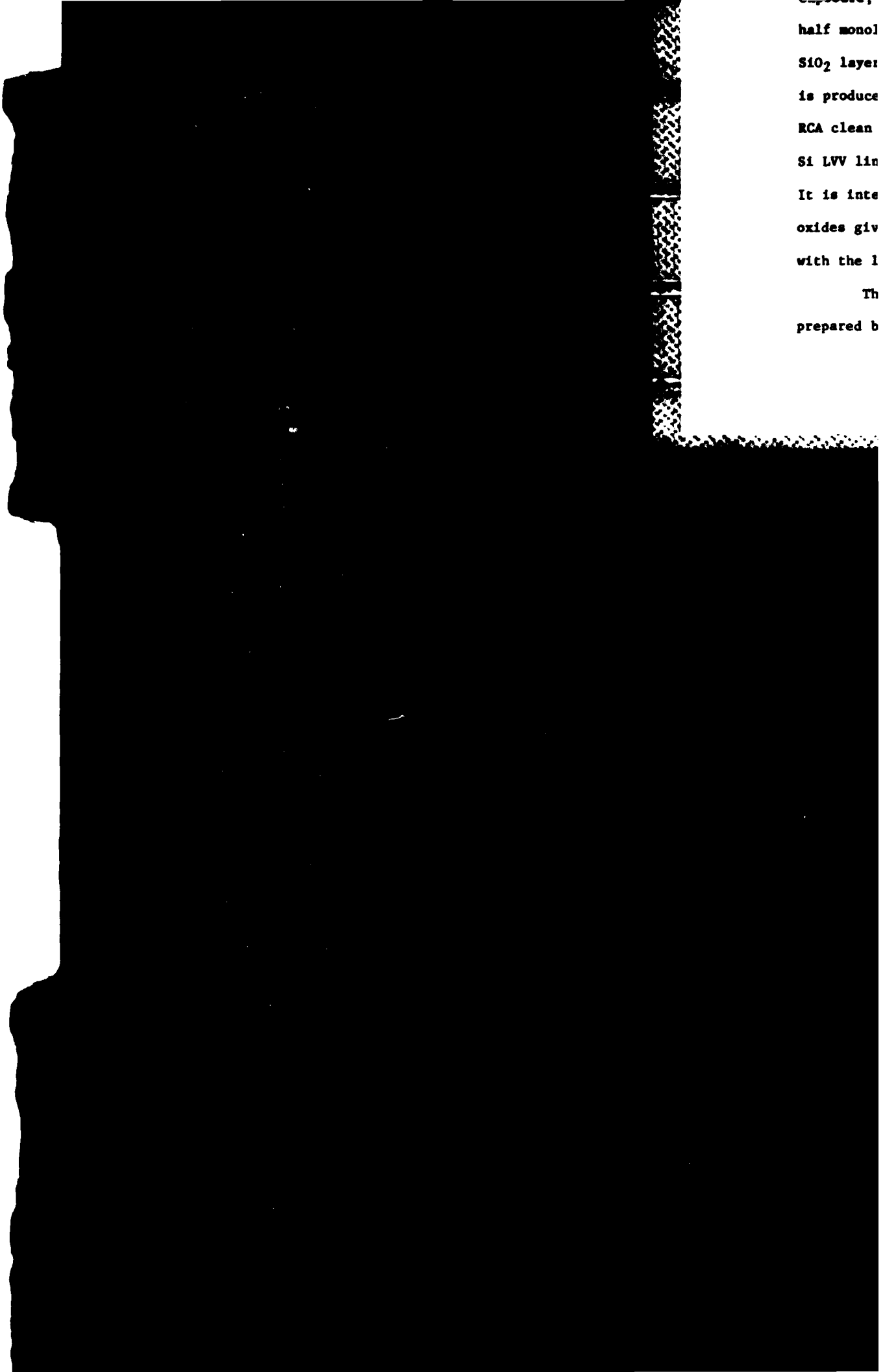

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